Claims

1. A reception circuit characterized by having:

a low noise amplifier having a low noise amplifying circuit with a low gain and a low noise amplifying circuit with a high gain which are capable of selective operation in accordance with control of a bias current; and

a quadrature demodulator connected with a serial capacitance to an output of said low noise amplifying circuit with the high gain of said low noise amplifier and directly connected to an output of said low noise amplifying circuit with the low gain.

2. The reception circuit according to Claim 1, characterized in that:

during operation of said low noise amplifying circuit with the high gain, a DC bias current thereof is passed independently of a DC bias current of said quadrature demodulator, and

during operation of said low noise amplifying circuit with the low gain, a DC bias current thereof is shared with the DC bias current of said quadrature demodulator.

3. The reception circuit according to Claim 1, characterized in that:

each of said low noise amplifying circuit with the high gain and said low noise amplifying circuit with the low gain has a pair of differentially connected transistors, and

a first and a second inductive elements are connected in series between emitters of the pair of transistors in said low noise amplifying circuit with the low gain, and both ends thereof are connected to emitters of the pair of transistors in said low noise amplifying circuit with the high gain through a third and a fourth inductive elements, respectively.

4. The reception circuit according to Claim 3, characterized in that:

said first to fourth inductive elements are formed of a single inductor in which a spiral is smaller helically from a first terminal in an outermost portion and then the spiral is larger through gaps of the helicity, and returns to a second terminal in the outermost portion, and a third and a fourth terminals are drawn from two positions in the middle between an innermost portion of the inductor and said first and second terminals, a fifth terminal is drawn from a position in the innermost portion, said first and second terminals are connected to the emitters of the pair of transistors in said low noise amplifying circuit with the low gain, said third and fourth terminals are connected to the emitters of the pair of transistors in said low noise amplifying circuit with the high gain, and said fifth terminal is grounded through a resistance.

5. The reception circuit according to Claim 3, characterized in that:

said quadrature demodulator has two Gilbert Cell circuits for an I channel and a Q channel, respectively,

and a current source for providing a current bias current for each of the Gilbert Cell circuits,

a first Gilbert Cell circuit has a first differential pair of transistors and a second differential pair of transistors, emitters of the first differential pair of transistors are directly coupled and selectively connected to said own current source and a collector of one of the pair of transistors in said low noise amplifying circuit with the low gain, and emitters of the second differential pair of transistors are directly coupled and selectively connected to said own current source and a collector of the other of the pair of transistors in said low noise amplifying circuit with the low gain, and

a second Gilbert Cell circuit has a third differential pair of transistors and a fourth differential pair of transistors, emitters of the third differential pair of transistors are directly coupled and selectively connected to said own current source and a collector of one of the pair of transistors in said low noise amplifying circuit with the low gain, and emitters of the fourth differential pair of transistors are directly coupled and selectively connected to said own current source and a collector of the other of the pair of transistors in said low noise amplifying circuit with the low gain.

6. The reception circuit according to Claim 4, characterized in that said reception circuit is configured with an IC chip.

7. A wireless communication terminal apparatus characterized by having:

a low noise amplifier having a low noise amplifying circuit with a low gain and a low noise amplifying circuit with a high gain which are capable of selective operation in accordance with control of a bias current;

a quadrature demodulator connected with a serial capacitance to an output of said low noise amplifying circuit with the high gain of said low noise amplifier and directly connected to an output of said low noise amplifying circuit with the low gain;

reception level detecting means for detecting a level of a reception signal; and

control means for performing control of said reception circuit in accordance with an output of said reception level detecting means, characterized in that:

said control means controls said low noise amplifier such that it operates the low noise amplifying circuit with the low gain when said reception signal level is high, and operates the low noise amplifying circuit with the high gain as said low noise amplifier when said reception signal level is low.

8. The wireless communication terminal apparatus according to Claim 7, characterized in that:

during operation of said low noise amplifying circuit with the high gain, a DC bias current thereof is passed independently of a DC bias current of said quadrature demodulator, and

during operation of said low noise amplifying circuit with the low gain, a DC bias current thereof is

shared with the DC bias current of said quadrature demodulator.

9. The wireless communication terminal apparatus according to Claim 7, characterized in that:

each of said low noise amplifying circuit with the high gain and said low noise amplifying circuit with the low gain has a pair of differentially connected transistors, and

a first and a second inductive elements are connected in series between emitters of the pair of transistors in said low noise amplifying circuit with the low gain, and both ends thereof are connected to emitters of the pair of transistors in said low noise amplifying circuit with the high gain through a third and a fourth inductive elements, respectively.

10. The wireless communication terminal apparatus according to Claim 9, characterized in that:

said first to fourth inductive elements are formed of a single inductor in which a spiral is smaller helically from a first terminal in an outermost portion and then the spiral is larger through gaps of the helicity, and returns to a second terminal in the outermost portion, and a third and a fourth terminals are drawn from two positions in the middle between an innermost portion of the inductor and said first and second terminals, a fifth terminal is drawn from a position in the innermost portion, said first and second terminals are connected to the emitters of the pair of transistors in said low noise amplifying circuit with the

low gain, said third and fourth terminals are connected to the emitters of the pair of transistors in said low noise amplifying circuit with the high gain, and said fifth terminal is grounded through a resistance.

11. The wireless communication terminal according to Claim 9, characterized in that:

said quadrature demodulator has two Gilbert Cell circuits for an I channel and a Q channel, respectively, and a current source for providing a current bias current for each of the Gilbert Cell circuits,

a first Gilbert Cell circuit has a first differential pair of transistors and a second differential pair of transistors, emitters of the first differential pair of transistors are directly coupled and selectively connected to said own current source and a collector of one of the pair of transistors in said low noise amplifying circuit with the low gain, and emitters of the second differential pair of transistors are directly coupled and selectively connected to said own current source and a collector of the other of the pair of transistors in said low noise amplifying circuit with the low gain,

a second Gilbert Cell circuit has a third differential pair of transistors and a fourth differential pair of transistors, emitters of the third differential pair of transistors are directly coupled and selectively connected to said own current source and a collector of one of the pair of transistors in said low noise amplifying circuit with the low gain, and emitters of the fourth differential pair of transistors are

directly coupled and selectively connected to said own current source and a collector of the other of the pair of transistors in said low noise amplifying circuit with the low gain, and

said control means makes said current source for each of said first and second Gilbert Cell circuit active when said low noise amplifying circuit with the high gain operates and inactive when said low noise amplifying circuit with the low gain operates.

12. The wireless communication terminal apparatus according to Claim 10, characterized in that said reception circuit is configured with an IC chip.